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SPECIFICATION

INVENTION:

METHOD AND APPARATUS FOR CONTROLLING
THICKNESS UNIFORMITY OF ELECTROPLATED LAYER

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METHOD AND APPARATUS FOR CONTROLLING THICKNESS
UNIFORMITY OF ELECTROPLATED LAYER

[0001] This application claims the priority of U.S. provisional application no. 60/256,924, filed December 21, 2000, the disclosure of which is expressly incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention generally relates to electrodeposition process technology and, more particularly, to an electrodeposition process and apparatus that yield planar deposition layers.

Description of Related Art

[0003] A conventional semiconductor device generally includes a semiconductor substrate, usually a silicon substrate, and a plurality of sequentially formed dielectric interlayers, such as silicon dioxide interlayers, and conductive paths or interconnects made of conductive materials. The interconnects are usually formed by filling a conductive material in trenches etched into the dielectric interlayers. In an integrated circuit, multiple levels of interconnect networks laterally extend with respect to the substrate surface. The interconnects formed in different layers can be electrically connected using vias or contacts.

A conductive material filling process of filling such features, i.e. via openings, trenches, pads or contacts, can be carried out by depositing a conductive material over the substrate including such features. Excess conductive material on the substrate can then be removed using a planarization and polishing technique such as chemical mechanical polishing (CMP).

[0004] Copper (Cu) and Cu alloys have recently received considerable attention as interconnect materials because of their superior electromigration and low resistivity characteristics. The preferred method of Cu deposition is electrodeposition. During fabrication, copper is electroplated or electrodeposited on substrates that are previously coated with barrier and seed layers. Typical barrier materials generally include tungsten (W), tantalum (Ta), titanium (Ti), their alloys and their nitrides. A typical seed layer material for copper is usually a thin layer of copper that is CVD or PVD deposited on the aforementioned barrier layer.

[0005] There are many different Cu plating system designs. For example, U.S. Patent No. 5,516,412, issued on May 14, 1996 to Andricacos et al., discloses a vertical paddle plating cell that is configured to electrodeposit a film on a flat article. U.S. Patent No. 5,985,123, issued on Nov. 16, 1999 to Koon, discloses yet another vertical electroplating apparatus which

purports to overcome the non-uniform deposition problems associated with varying substrate sizes.

[0006] During the Cu electrodeposition process, specially formulated plating solutions or electrolytes are used. These solutions or electrolytes contain ionic species of Cu and additives to control the texture, morphology, and plating behavior of the deposited material. Additives are needed to make the deposited layers smooth and somewhat shiny.

[0007] Figures 1 through 2 exemplify a conventional electrodeposition method and apparatus. Figure 1A illustrates a substrate 10 having an insulator layer 12 formed thereon. Using conventional etching techniques, features such as a row of small vias 14 and a wide trench 16 are formed on the insulator layer 12 and on the exposed regions of the substrate 10. Typically, the widths of the vias 14 are sub-micronic. The trench 16 shown in this example, on the other hand, is wide and has a small aspect ratio. The width of the trench 16 may be five to fifty times or more greater than its depth.

[0008] Figures 1B-1C illustrate a conventional method for filling the features with copper material. Figure 1B illustrates that a barrier/glue or adhesion layer 18 and a seed layer 20 are sequentially deposited on the substrate 10 and the insulator 12. After depositing the seed layer 20, as shown in Figure 1C, a conductive material layer 22 (e.g., a copper layer) is partially electrodeposited thereon from a suitable plating bath or bath formulation. During this step,

an electrical contact is made to the copper seed layer 20 and/or the barrier layer 18 so that a cathodic (negative) voltage can be applied thereto with respect to an anode (not shown). Thereafter, the copper material layer 22 is electrodeposited over the substrate surface using plating solutions, as discussed above. By adjusting the amounts of the additives, such as chloride ions, a suppressor/inhibitor, and an accelerator, it is possible to obtain bottom-up copper film growth in the small features.

[0009] As shown in Figure 1C, the copper material 22 completely fills the vias 14 and is generally conformal in the large trenches 16, because the additives that are used are not operative in large features. Here, the Cu thickness t_1 at the bottom surface of the trench 16 is about the same as the Cu thickness t_2 over the insulator layer 12. As can be expected, to completely fill the trench 16 with the Cu material, further plating is required. Figure 1D illustrates the resulting structure after additional Cu plating. In this case, the Cu thickness t_3 over the insulator layer 12 is relatively large and there is a step height s_1 from the top of the Cu layer on the insulator layer 12 to the top of the Cu layer 22 in the trench 16. For IC applications, the Cu layer 22 needs to be subjected to CMP or other material removal processes so that the Cu layer 22 as well as the barrier layer 18 on the insulator layer 12 are removed, thereby leaving the Cu layer

only within the features 14 and 16. These removal processes are known to be quite costly.

[0010] Methods and apparatus to achieve a generally planar Cu deposit as illustrated in Figure 1E would be invaluable in terms of process efficiency and cost. The Cu thickness t_5 over the insulator layer 12 in this example is smaller than the traditional case as shown in Figure 1D, and the step height s_2 is also much smaller than the step height s_1 . Removal of the thinner Cu layer in Figure 1E by CMP or other methods would be easier, providing important cost savings.

[0011] In U.S. Patent 6,176,992 B1 entitled "Method and Apparatus for Electrochemical Mechanical Deposition", commonly owned by the assignee of the present invention, an electrochemical mechanical deposition (ECMD) technique is disclosed that achieves deposition of the conductive material into cavities on a substrate surface while minimizing deposition on the field regions by polishing the field regions with a pad as the conductive material is deposited, thus yielding planar copper deposits. The plating electrolyte in this application is supplied to the small gap between the pad and the substrate surface through a porous pad or through asperities in the pad.

[0012] Co-pending U.S. Patent Application Serial No. 09/511,278, entitled "Pad Designs and Structures for a Versatile Materials Processing Apparatus" filed February 23, 2000, which is commonly owned by the assignee of the present

invention, describes various shapes and forms of holes in pads through which electrolyte flows to a wafer surface.

[0013] Another invention described in U.S. Patent Application Serial No. 09/740,701, entitled "Plating Method and Apparatus That Creates a Differential Between Additive Disposed on a Surface and a Cavity Surface of a Work Piece Using an External Influence", filed December 18, 2000, provides a method and apparatus for "mask-pulse plating" a conductive material onto a substrate by intermittently moving the mask, which is placed between the substrate and the anode, into contact with the substrate surface and applying power between the anode and the substrate during the process. Yet another invention described in U.S. Patent Application Serial No. 09/735,546, entitled "Method of and Apparatus for Making Electrical Contact to Wafer Surface For Full-Face Electroplating or Electropolishing", filed December 14, 2000, provides complete or full-face electroplating or electropolishing of the entire wafer frontal side surface without excluding any edge area for the electrical contacts. This method uses an anode having an anode area, and electrical contacts placed outside the anode area. During the process, the wafer is moved with respect to the anode and the electrical contacts such that a full-face deposition over the entire wafer frontal surface is achieved. Another non-edge-excluding process described in U.S. Patent Application Serial No. 09/760,757, entitled "Method and Apparatus for

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Electrodeposition of Uniform Film with Minimal Edge Exclusion on Substrate", filed January 17, 2001, also achieves full-face deposition with a system having a mask or a shaping plate placed between the wafer frontal surface and the anode. The mask contains asperities allowing electrolyte flow. In this system, the mask has a larger area than the wafer surface. The mask is configured to have recessed edges through which electrical contacts can be contacted with the front surface of the wafer. In this system, as the wafer is rotated, the full surface of the wafer contacts with the electrolyte flowing through the shaping plate, achieving deposition.

[0014] Figure 2A shows a schematic depiction of a prior art electrodeposition system 30. In this system, a wafer 32 is held by a wafer holder 34 with the help of a ring clamp 36 covering the circumferential edge of the wafer 32. An electrical contact 38 is also shaped as a ring and connected to the (-) terminal of a power supply for cathodic plating. The wafer holder 34 is lowered into a plating cell 40 filled with plating electrolyte 42. An anode 44, which makes contact with the electrolyte 42, is placed across from the wafer surface and is connected to the (+) terminal of the power supply. The anode 44 may be made of the material to be deposited, i.e. copper, or may be made of an appropriate inert anode material such as platinum, platinum coated titanium or graphite. A plating process commences upon application of power. In this plating system, the electrical contact 38 is

sealed from the electrolyte and carries the plating current through the circumference of the wafer 32.

[0015] Figures 1A through 1E show how the features on the wafer surface are filled with copper. For this filling process to be efficient and uniform throughout the wafer, it is important that a uniform thickness of copper be deposited over the whole wafer surface. Also, the resulting thickness uniformity of the plating process, i.e. the uniformity of thickness t3 in Figure 1D and the uniformity of the thickness t5 in Figure 1E, needs to be very good (typically less than 10% variation, and preferably less than 5% variation) because a non-uniform copper thickness causes problems during the CMP process.

[0016] As shown in Figure 2B, in order to improve uniformity of the deposited layers, shields 46 may be included in the prior art electroplating system such as that shown in Figure 2A. In such systems, either the wafer 32 or the shield 46 may be rotated. Such shields are described, for example, in U.S. Patent 6,027,631 to Broadbent, U.S. Patent 6,074,544 to Reid et al., and U.S. Patent 6,103,085 to Woo et al. Further, in such systems, electrical thieves can be used for electrodepositing materials. Such thieves are described, for example, in U.S. Patents 5,620,581 and 5,744,019 to Ang, U.S. Patent 6,071,388 to Uzoh, and U.S. Patents 6,004,440 and 6,139,703 to Hanson et al.

[0017] In view of the foregoing, there is a need for alternative electrodeposition processes and systems that deposit uniform conductive films and have the ability to change deposition rates on various portions of a substrate during the deposition process.

SUMMARY OF THE INVENTION

[0018] In one aspect of the present invention, a system for electrodepositing a conductive material on a surface of a wafer is provided. The system includes an anode, a mask having upper and lower surfaces, a conductive mesh positioned below the upper surface of the mask or shaping plate, and an electrolyte. The mask includes a plurality of openings extending between the upper and lower surfaces, and the mask is supported between the anode and the surface of the wafer. The conductive mesh is positioned below the upper surface of the mask such that the plurality of openings of the mask defines a plurality of active regions on the conductive mesh. The conductive mesh is connected to a first electrical power input. The liquid electrolyte flows through the openings of the mask and through the active areas of the mesh so as to contact the surface of the wafer.

[0019] Another feature of the invention is the provision of an apparatus which can control thickness uniformity during deposition of conductive material from an electrolyte onto a surface of a semiconductor substrate. The apparatus includes

an anode which can be contacted by the electrolyte during deposition, a cathode assembly including a carrier adapted to carry the substrate for movement during deposition, a conductive element permitting electrolyte flow therethrough, and a mask lying over the conductive element. The mask has openings, permitting electrolyte flow therethrough, which define active regions of the conductive element by which a rate of conductive material deposition onto the surface can be varied. A power source can provide a potential between the anode and the cathode assembly so as to produce the deposition.

[0020] Preferably, the conductive element is a conductive mesh, and includes a plurality of electrically isolated sections. At least one isolation member or gap can separate the electrically isolated sections. The electrically isolated sections can be connected to separate control power sources.

[0021] In one configuration, the conductive element can be sandwiched between top and bottom mask portions which together define the mask. The conductive element could be placed under a lower surface of the mask. One of the electrically isolated sections may circumferentially surround another of the electrically isolated sections.

[0022] The electrically isolated sections could be irregularly shaped. Alternatively, one of the electrically isolated sections can be ring shaped while the other of these

sections is disc shaped. The electrically isolated sections could additionally define adjacent strips.

[0023] At least one control power source can be used to supply a voltage to at least one of the electrically isolated sections to vary the rate of conductive material deposition onto a region of the substrate surface. In one configuration, the rate can be increased or decreased. Apparatuses such as those mentioned can be used to control thickness uniformity during conductive material deposition in a process including contacting the anode with the electrolyte, providing a supply of the electrolyte to the substrate surface through the conductive element and through the mask lying over the conductive element, providing a potential between the anode and the surface, and supplying a voltage to the conductive element in order to vary the conductive material deposition rate.

[0024] Uniform electroetching of conductive material on the wafer surface by reversing polarities of the anode and the cathode assembly is also within the scope of this invention. A process for establishing a relationship between deposition currents in active regions on the conductive mesh and thicknesses of the conductive material deposited onto the semiconductor substrate surface is also contemplated.

[0025] These and other features, aspects and advantages of the present invention will become better understood with reference to the drawings and the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] Figure 1A is a partial sectional view of a semiconductor substrate with an overlying insulator layer including trenches and vias.

[0027] Figures 1B and 1C are cross sectional views illustrating a conventional method for filling trenches and vias, such as those of Figure 1A, with a conductive material.

[0028] Figure 1D is a cross sectional view showing a structure similar to that of Figure 1C but after additional conductive material deposition.

[0029] Figure 1E is a view similar to Figure 1D but showing a structure with a reduced conductive material thickness over an insulator layer.

[0030] Figure 2A is a schematic illustration, in cross section, of a known electrodeposition system.

[0031] Figure 2B is a schematic illustration similar to Figure 2A but showing a system which includes shields intended to improve deposition uniformity.

[0032] Figure 3 is a schematic cross sectional illustration of one embodiment of an electrodeposition system according to this invention.

[0033] Figure 4 shows the system of Figure 3 when used to provide substantially flat conductive material deposition.

[0034] Figure 5 is a top plan view of a conductive mesh, with irregularly shaped electrically isolated sections, which can be used in the embodiment of Figures 3 and 4.

[0035] Figure 6A is an enlarged cross sectional view showing a combined mask and mesh structure in proximity with a front surface of a semiconductor substrate.

[0036] Figure 6B is an enlarged view of section 6B appearing in Figure 6A.

[0037] Figure 6C is a partial plan view along line 6C-6C of Figure 6B.

[0038] Figure 7 shows another embodiment of a combined mask and mesh structure.

[0039] Figure 8A is a top plan view of a conductive mesh similar to that of Figure 5 but in which the electrically isolated sections are not irregularly shaped.

[0040] Figure 8B shows the mesh of Figure 8A as sandwiched between top and bottom mask portions in proximity with a front surface of a semiconductor substrate.

[0041] Figure 9A is a top plan view of a conductive mesh with electrically isolated sections which define adjacent strips.

[0042] Figure 9B is a view similar to that of Figure 8B but showing the mesh of Figure 9A as sandwiched between top and bottom mask portions.

[0043] Figure 9C is a plan view along line 9C-9C of Figure 9B.

[0044] Figure 10 is a schematic illustration of one system by which a mesh in accordance with any of the previously described embodiments can be energized.

[0045] Figure 11 is a schematic illustration of another system in which multiple meshes are multiplexed through multiple switches.

[0046] Figure 12 is an enlarged view of part of the system shown in Figure 11.

[0047] Figure 13 is a view similar to Figure 12 showing a switch in a position by which copper is plated from a mesh onto a wafer as well as from an anode onto the wafer.

[0048] Figure 14 is a view similar to Figure 13 but showing the switch in a position by which copper is plated to the mesh so that less plating occurs on the wafer.

[0049] Figure 15 is a schematic illustration of another system which can be used to correlate plating current to plated metal thickness measurements.

DETAILED DESCRIPTION OF THE INVENTION

[0050] The present invention provides a method and a system to control the uniformity of a conductive material layer deposited on a surface of a semiconductor. The invention can be used with ECMD, mask pulse plating and full face plating as

well as plating systems that deposit conformal films. The deposition process of the present invention advantageously achieves deposition of a conductive material in a plurality of cavities, such as trenches, vias, contact holes and the like, on a surface of a semiconductor wafer.

[0051] As is known, during an electrodeposition process of a surface of a wafer, the current density applied to the surface is substantially greater at the periphery of the surface than the center of the surface. In the prior art, this higher current density results in an increased deposition rate of the deposited film at the periphery of the wafer as compared to the wafer center. With the present invention, the film thickness difference between the interior and the periphery of the wafer may be eliminated with use of the combination of the perforated plate or a mask and a conductive mesh of the present invention during the electrodeposition. The combination of the perforated plate and the conductive mesh facilitates uniform deposition of the conductive material.

[0052] Further, in another embodiment, the present invention achieves deposition of the conductive material through the combination of the perforated plate and the conductive mesh into the features of the surface of the wafer while minimizing the deposition on the top surface regions between the features by contacting, sweeping and/or polishing of the surface with the perforated plate of the present

invention. For systems that can deposit planar films, i.e., ECMD, mask pulse plating and full face plating, the thickness uniformity can be controlled to a certain extent through designing the shape, size and location of the openings in the mask, pad or shaping plates that are employed. Although effective for a given process parameters, such approaches may not be flexible enough to have a dynamic control over the uniformity of the deposition process.

[0053] The apparatus and the process of the present invention exhibit enhanced deposition characteristics resulting in layers having flatness previously unattainable and conductive layers with materials characteristics surpassing that of prior art layers that have been produced using prior art processes and devices.

[0054] Reference will now be made to the drawings wherein like numerals refer to like parts throughout. As shown in Figure 3, an electrodeposition system 100 of the present invention may preferably comprise a cathode assembly 102 and an anode assembly 104. The system 100 may be used to deposit a conductive material such as copper on a semiconductor wafer such as silicon wafer. Although copper is used as an example, the present invention may be used for deposition of other common conductors such as Ni, Pd, Pt, Au and their alloys. The cathode assembly 102 of the electrodeposition system 100 may be comprised of a wafer carrier 106, shown in Figure 3 holding an exemplary wafer 108, which is attached to a carrier

arm 110. The carrier arm may rotate or move the wafer 108 laterally or vertically.

[0055] The anode assembly 104 of the system 100 may be comprised of an anode 112, preferably a consumable copper anode, a mask, and a conductive mesh 115 of the present invention. The mask, as shown, is in the form of a mask plate 114. The anode 112 may preferably be placed into an enclosure such as an anode cup 116 which may be enclosed by the mask plate 114 and the conductive mesh 115 as in the manner shown in Figure 3. The mask plate 114 and the mesh 115 are both perforated plates. The mask plate preferably comprises a first mask portion 114a or a top mask portion and a second mask portion 114b or a bottom mask portion. The mesh 115 may be interposed or sandwiched between the top and bottom portions 114a, 114b. The mask plate 114 may comprise a plurality of openings or asperities 117 which allow a copper plating electrolyte 118 to flow through the mask plate 114 and the mesh 115, and wet the front surface 108a of the wafer 108 and deposit material on the front surface 108a of the wafer under applied potential. The asperities 117 in the top and bottom mask portions may generally be aligned to allow electrolyte flow through the top and bottom mask portions 114a, 114b. However, their partial alignment or placement in any other way that still allows electrolyte flow through the top mask portion 114a to the wafer surface is also within the scope of this invention. During the electrodeposition

process, the wafer surface 108a may be kept substantially parallel to an upper surface 119 of the mask plate 114 and rotated. It should be understood that what counts is the relative motion between the wafer surface and the pad surface. This motion can be a rotational motion or a rotation motion with linear translation.

[0056] The mesh 115 may have first and second sections 115a and 115b that are electrically isolated from each other by an isolation member 115c. The isolation member 115c may be a gap separating both sections. The first section 115a may be connected to a first control power source V1 and the second section may be connected to a second control power source V2. If the control power supplies in part a negative voltage on the mesh sections, this results in some material deposition on the sections 115a and 115b during the electrodeposition, i.e. some deposition is "stolen" directly across from these sections. On the other hand, if a positive voltage is applied to the mesh with respect to the wafer surface, the section of the wafer across from the section of the mesh with positive voltage receives more plating. As will be described below, with the applied power V1 and in combination with the functionalities of the mask asperities, the first section of the mesh 115^a may, for example, control the thickness at the periphery of the of the front surface 108a of the wafer 108. In this respect, the second power V2 on the second section 115a controls the thickness on the center or near center

115a
115b

[0058] Figure 5 exemplifies the conductive mesh 115 and the sections 115a and 115b separated by the isolation member 115c. The mesh 115 comprises openings 126 allowing electrolyte to flow through the openings. The mesh 115 may be made of platinum or platinum coated titanium mesh or other inert conductive materials. After a cycle of 5 to 50 uses, the polarity of the system may be reversed and the mesh can be cleaned for another cycle of uses. The number of possible cycles, before cleaning, depends on the use of the mesh and the size of the mesh. Although two regions are shown in Figure 5, the use of more than two regions is within the scope of this invention.

[0059] As shown in Figures 6A-6C, the mesh 115 may be placed between the top and bottom mask portions 114a, 114b using suitable fastening means or may be formed as an integral part of the mask 114. As shown in Figures 6B-6C, in side view and plan view respectively, when the mesh 115 and the mask 114 are combined, the openings 117 through the mask 114 define a plurality of active regions 130 on the mesh 115. During electrodeposition, when a negative potential is applied to the mesh 115, material deposition onto the active regions 130 occurs. If a positive voltage is applied, the active regions 130 of the mesh 115 become anodic and cause additional deposition on the wafer surface right above them. By varying the size and shape of the openings 117, the size and shape of the active regions 130 are changed. This, in turn, varies the

deposition rates on the front surface 108a of the wafer 108 and hence alternatively controls the film thickness.

[0060] Figure 7 illustrates another embodiment of a combined structure of the mask 114 and the mesh 115. In this embodiment, the mesh 115 is placed under a lower surface 128 of the mask plate 114. It is also within the scope of the present invention to position a plurality of meshes between the upper surface 119 and the lower surface 128 of the mask 114. Each of a plurality of meshes may be isolated from each other with a layer of mask, and each mesh may have a sequentially applied different power during the electrodeposition process to control the deposition rate.

[0061] Figures 8A and 8B show another embodiment of the conductive mesh. In this embodiment, a mesh 131 comprises a first section 131a and a second section 131b isolated from one another by an isolation member 131c. The first section 131a is ring shaped and is fed by a first control power V1. As shown in Figure 8B, the first section 131a controls the deposition thickness at a periphery 132 of the wafer 108. The second section 131b, which is disc shaped, controls the deposition thickness at the center 134 of the wafer 108 by a second control power V2.

[0062] Figure 9A-9C show another embodiment of a mesh 136 comprising a first section 136a and a second section 136b isolated from one another by an isolation member 136c. The first and second sections 136a, 136b are both strip shaped and

may be used with a mask 138, which may have a circular or rectangular shape, having openings 140. Similar to the previous embodiments, the mask 138 may comprise a top portion 138a and a bottom portion 138b, and the mesh 136 may be sandwiched between the top and bottom portions 138a, 138b. As shown in Figures 9B and 9C, the first section 136a is aligned with a first end 142 of the mask 138 to control the deposition thickness at the periphery 132 of the wafer 108 which rotates during the electrodeposition process. The wafer 108 may be also moved in the direction Y. Similarly, the second section 136b is aligned with the center 144 of the mask 138 to control the deposition thickness of the center 134 of the wafer 108.

[0063] Of course, a uniform electroetching of the wafer surface by reversing polarities of the system 100 described above is also within the scope of this invention.

[0064] Figure 10 shows one embodiment of energizing the sections of the mesh described in the previous embodiments. In this embodiment, an exemplary mesh 150 may be interposed between a top portion 152a and a bottom portion 152b of a mask plate 152. The mask plate 152 comprises a plurality of asperities 154 defining active areas 156 on the mesh 150. The mesh comprises a first or peripheral section 150a and a second or central section 150b which are isolated from one another by an isolation member 150c. A first power source Va is connected to a wafer 158, having a conductive surface 158a and an anode of an anode cup (not shown) of an electrodeposition

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system such as those described with regard to Figures 3-4. The first power source Va may also be connected to the first section 150a or the second section 150b of the mesh 150 through a switch S2. A second power source Vb is connected to the wafer 158 and the first section 150a or the second section 150b of the mesh 150 through the switch S1.

[0065] Accordingly, if the switch S1 connects node D to node A, no voltage is applied to the mesh 150. If the switch S1 connects node D to node B, a positive voltage is applied to the section 150a of the mesh 150. Accordingly, additional deposition is achieved in the section or sections AA on the wafer surface 158a. Each section AA is positioned right across from a section 150a of the mesh 150. If the switch S1 connects node D to node C, the section BB on the wafer receives the additional deposit.

[0066] If the switch S2 connects node H to node E, regular deposition commences on the wafer surface 158a. If switch S2 connects node H to node G, section 150a of the mesh 150 is rendered cathodic, and therefore attracts deposition, reducing the amount of deposit on the section AA of the wafer surface 158a. Similarly, if S2 connects node H to node F, deposition on the section BB of the wafer surface 158a is reduced. Thus, the deposition rates in both sections AA and BB of the wafer can be controlled by selecting the proper positions for the switches S1 and S2.

[0067] Only one power supply is required if one multiplexes the meshes $M_1, M_2, M_3 \dots M_n$ through switches $S_1, S_2, S_3 \dots S_n$ as shown in Figures 11-14. Also, measuring the current through a series of resistors would be useful for designing better mask patterns in the system. This is especially required for the present cell design because it is a complex cell to computer model and the potential field is not uniform across the system.

[0068] Everything can be done with one power supply if many switches are used. For example, looking at one macro-plating cell M_1 as shown in Figures 11-14, in one case, shown in Figure 13, when the switch S_1 is switched to the V_A position, mesh M_1 is at potential V_A , and copper plates both from the mesh to the cathode and from the anode to the cathode.

[0069] When the switch S_1 is switched to the V_C position as shown in Figure 14, the mesh M_1 is at a cathode position and copper substantially plates to the mesh. To control thicknesses on different sections of the wafers, the duty cycles of switched meshes can be modulated in these regions.

[0070] If the switch S_1 is in the not connected (N_C) position, and is not connected to V_A or V_C , then copper will plate as in a normal system.

[0071] Substantially isolated meshes, one for each opening in the mash, can also be used to determine the local current density of each opening in the mesh. Measuring this is helpful in designing and testing new mask patterns to get

optimized or better control on the plated thickness uniformity.

[0072] For one cell, referring to Figure 15, in a first step, the voltage drop across the R_1 resistor is determined and the plating current for the particular cell is determined. This operation is then repeated in subsequent steps for every cell. Results are then mapped and compared to plated metal thickness measurements.

[0073] It should be understood, of course, that the foregoing relates to preferred embodiments of the invention and that modifications may be made without departing from the spirit and scope of the invention as set forth in the following claims.